CENTERING AND TOLERANCING THE COMPONENTS OF MICROWAVE AMPLIFIERS

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Abstract

A simple graphical statistical method of circuit design centering and tolerancing for a desired circuit manufacturing yield is presented. The method is iterative and based on a parametric study of circuit yield estimates using Monte Carlo circuit analysis. Circuit elements including device s-parameters and distributed parameters as well as lumped components are considered. An application of this method is given in an example.

INTRODUCTION

Most microwave amplifiers are built in a production environment. It is the responsibility of the designer to provide a design that can be built with high yield. This means the designer must take into account the effects that component and process tolerances will have on the performance of the circuit. A number of CAD (1, 2, 3) programs will provide an estimate of yield if tolerances are known. We have found that the yield predicted for standard tolerances is frequently too low, and therefore, it is necessary to determine which tolerances to tighten. None of the CAD packages provides a good solution to the problem of determining the center values and tolerances that will provide acceptable yield.

We provide a method of determining these tolerances. The method, which is based on a graphical presentation of the results of computer simulation, provides good insight into the interaction of center values and of tolerances. Even when the simulation is done on a personal computer, the variation in 25 or more parameters that specify lumped elements, transistors (s-parameters) and distributed elements, can be studied in a few hours.

Gupta, et. al. (4) Antreich and Koblitz (5), and Voreadis and Mayne (6) have discussed design centering and tolerancing. None of these authors

provides, as we do, a general algorithm for the selection of center values and tolerances that can be implemented on a small computer. The same comment applies to the work of Elias (7) and Bandler (8, 9). The subject of selecting component values has a jargon that may not be familiar to microwave circuit designers. The terms design centering and design tolerancing are used. Design centering refers to the determination of nominal values for the design. Design tolerancing refers to the selection of tolerances about the nominal values. Subsequent sections of this paper present background on the selection of nominal values and tolerances, our method, an example to illustrate the method, and conclusions.

Background

Early in the design of an amplifier, the designer will decide on a tentative circuit configuration and a tentative list of components. Preliminary design work often uses graphical techniques based on the Smith Chart. Once a trial circuit is available, CAD tools are used to determine the set of component values that provide the best compromise between requirements and attainable performance. If an acceptable design is achieved, the designer can go on to subsequent steps, otherwise the circuit is revised and the process is repeated.

The CAD routines used to obtain the nominal component values are frequently called optimizers. This is misleading because the routines search for a set of component values that minimize, in the least squares sense, the difference between the specified performance and the calculated performance of the circuit. If there is only one set of component values for which the calculated performance is acceptable, it will be almost impossible to build the circuit in a production environment. This means that the requirements on the circuit have to be less stringent than what could be achieved with a perfectly matched set of components. How do the CAD routines take

this into account? They do not. They will provide a set of component values for which the calculated performance matches the specified performance, but it is unlikely that this set will consist of the values that will result in highest yield. This is not a fault of the routines, it is a result of the fact that high yield in the presence of tolerances is not a criteria used in the selection of the component values. We have found it convenient to use the set of values obtained from a CAD "optimizer" as the starting point for our algorithm.

It is important to be sure that the design specifications provide a balanced set of requirements. For example, if an amplifier consistently meets requirements for gain and output return loss, but fails a requirement for input return loss, redesign of the input stage rather than the specification of tight tolerances will probably result in a more manufacturable design.

The Design Approach

Consider a circuit performance function $G(X)$ which depends on a set of parameter values $X = (x1, x2, \ldots xn)$. No assumptions are needed on the form of $G(X)$. Let PHI be the region of G in which the circuit meets all its performance specifications. A circuit with parameters X is accepted if:

$$G(X) \in PHI$$

Let R be the region of acceptable parameter values. Then:

$$G(X) \in PHI \quad implies \quad X \in R$$

The parameter values vary randomly with a probability density function (pdf) $p(X)$. Thus, the manufacturing yield Y is defined as (5):

$$Y = \int_R p(X)dX$$

Another useful formulation of Y involves the acceptance function $del(X)$ defined as:

$$del(X) = \begin{cases} 1 \text{ if } G(X) \in PHI : \text{good circuit} \\ 0 \text{ if } G(X) \notin PHI : \text{bad circuit} \end{cases}$$

Now Y can be expressed as the expected value of $del(X)$:

$$Y = \int del(X)p(X)dX$$

Suppose that m circuits are constructed using components drawn randomly from their manufacturing distributions. Then an unbiased estimator of Y is:

$$\tilde{Y} = \frac{1}{m} \sum_{i=1}^{m} del(Xi) = \frac{n}{m}$$

Where n is the number of circuits which are accepted. The yield could be estimated from electrical test results if a large number of circuits were built. Another approach, which is much cheaper, is to perform repeated network analysis with random choices of the component values. This numerical approach is an example of a Monte Carlo analysis. The most common use of Monte Carlo analysis is to estimate the yield, given the distribution of component values. However, our problem is to determine nominal values and ranges for component values for which the yield is sufficiently high.

This problem is not straightforward and is not solved with any available software packages. The computation of the yield factors and their graphical displays is the essence of our solution to the problem. The yield factor $Y(xi)$ is the yield with all component values varied randomly over their ranges, except for the ith component which is fixed at the value xi. That is:

$$Y(xi) = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} del(X)p(X)dx1,dx2,\ldots,dxi-1, dxi+1,\ldots,dxn.$$

If $Y(xi)$ is essentially constant for all xi in the range of the ith component value, then the yield Y is not sensitive to the ith component. It is important to realize that $Y(xi)$ may change if any of the ranges or distributions of the other variables change. If the overall yield Y is less than the acceptable yield, and $Y(xi)$ is low, the yield is improved by eliminating the value xi from the range of the ith component. The yield factors for all other components may not be improved, iteration may be required.

An unbiased estimate of the yield factor can be computed from a Monte Carlo simulation:

$$\tilde{Y}(xi) = \frac{1}{m} \sum_{j=1}^{m} del(Xj)$$

where the ith component of X is fixed at xi.

The sum is over all values of X which have the ith component equal to xi, and m is the number of such values of X.

It is usually satisfactory to divide the ranges for the components into ten equal regions, and to place the nominal value between regions five and six. An approximation to $Y(xi)$ is computed from the results of 1000 Monte Carlo runs in which all parameters of interest are allowed to vary. A priori information about the distributions of parameter values and about correlation between values is used in the Monte Carlo process.

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If there are ten regions and 2000 runs, each summation for the calculation of Y(xi) will contain approximately 100 values. We have found that 100 runs produce an adequate estimate of Y(xi). In our experience, 1000 analyses of a four-transistor circuit can be completed in one-to-two hours on a high-performance personal computer.

We let all of the parameters of interest vary in all of the Monte Carlo simulations. It might seem advantageous to first identify and then eliminate from consideration the parameters that have little effect on the yield and then concentrate on the ones that have a large effect. However, we have found the yield factor histograms themselves best identify the parameters that have little effect on yield. Elimination of these parameters from the second and later iterations of the Monte Carlo process would make these simulations less realistic and would save very little computer time as most of this time is spent in circuit analysis. However, after the second iteration, we usually only plot the histograms for the components of interest.

Tolerancing and Design Centering

The key to the success of our method is a straightforward graphical display of the yield factor. For each parameter, a histogram is presented which shows the calculated yield factor for each component value region. The adjustments to the center value and tolerance limits are made as follows.

Step 1 If the histogram is not symmetric about the chosen nominal value, the nominal value should be moved to make the curve symmetric. This is essentially a design centering step.

Step 2 If the histogram shows low yield factors at the parameter limits, the limits are tightened.

These two steps are iterative. After the tolerances and nominal values are adjusted, the Monte Carlo procedure is repeated and the histograms of yield factors are again plotted. Further adjustments are made if necessary. In our experience, two or three iterations are generally sufficient.

The centering and tolerancing procedure we have described does not take into account cost. This is not an oversight. In our experience, once an engineer has the histograms, the engineer is able to make cost effective choices.

Example

A representative amplifier circuit is shown in Figure 1 (11). The circuit requirements are 15 dB gain and S11 < -10 dB from 8 to 12 GHz. The nominal values for the circuit were determined with Touchstone software (3).
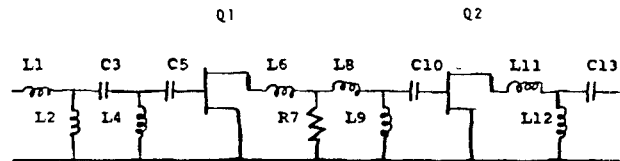

Figure 1 The Amplifier Circuit

Initial values for the components are shown in Figure 2. Capacitances are in pF, inductances in nH, resistances in ohms, and S-parameters are referred to Z = 50 Ohms.

L1	0.47	L2	4.94
C3	0.29	L4	0.48
C5	7.04	L6	0.06
R7	500	L8	1.01
L9	2.08	C10	0.58
L11	1.15	L12	0.69
C13	2.28		

Q1 and Q2 (Ref.11)

f	S11		S21	
GHz	Mag.	Phase	Mag.	Phase
8	0.775	-107	1.96	90
9	0.75	-118	1.84	81
10	0.73	-128	1.73	73
11	0.71	-136	1.64	64
12	0 695	-145	1.55	56

f	S12		S22	
GHz	Mag.	Phase	Mag.	Phase
8	0.035	104	0.735	-42
9	0.040	110	0.74	-47
10	0.050	114	0.75	-52
11	0.053	115	0.755	-58
12	0.060	115	0.765	-62

Figure 2. Initial Compomnent Values

This circuit was analyzed for yield with +- 10% variation on all component values (including transistor s-parameters). The yield was 73%. The yield factor curves were then calculated for each component. The curves for components L1, C3, and L4 are shown in Figure 3. The curve for component L1 is typical of most curves, indicating that the nominal value and the tolerance are satisfactory. An examination of the curve for component C3 shows that the nominal value should be raised by about 2% and the tolerance should be lowered to about +- 5%.
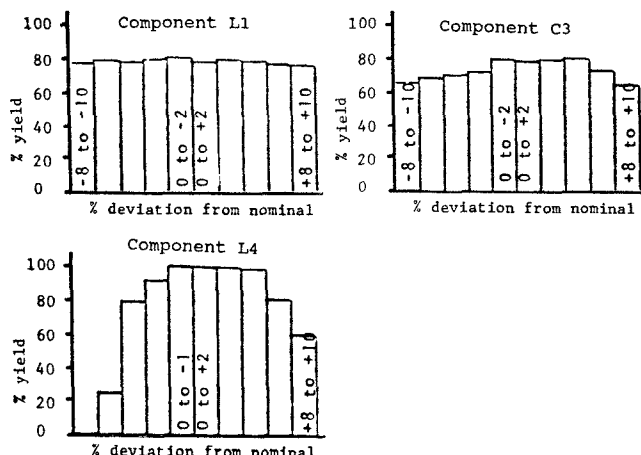
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Figure 3 Yield Factor Histograms For The Initial Component Values.

The following changes were made:
    Component C3, nominal value = .292
    Component L4, nominal value = .490
    Component L4, tolerance   = +- 5%
and the Monte Carlo procedure was repeated.
    The yield factor histograms for components C3 and L4 after the changes are shown in Figure 4. The yield is now 97%.
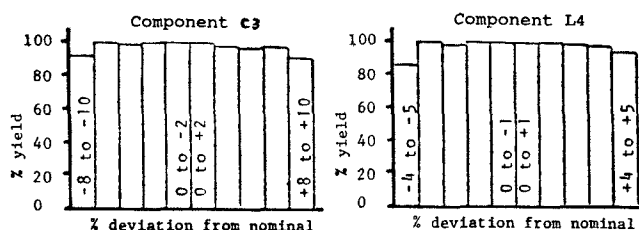

Figure 4 Yield Factor Histograms After The Changes Were Made.

Conclusions

The determination of center values and tolerances is an essential step in the design of an amplifier that will be built in production. The statistical analysis routines in some of the commercially available software packages provide valuable insight into the yield that can be expected for a given set of center values and tolerances but do not provide a convenient way to solve the inverse problem. We have shown that Monte Carlo simulation and yield factor histograms provide a straightforward way to determine center values and tolerances which will give a good manufacturing yield.

References

(1) Super Compact, Compact Software, 483 McLean Blvd., Paterson, NJ, 07540.

(2) S-Node, Suncrest Software, Veradale WA.

(3) Touchstone, EESof, 31194 La Baya Drive, Westlake Village, CA 91361.

(4) Gupta, K.C., Ramesh, G., and Rakesh, C., "Computer-Aided Design of Microwave Circuits," Artech House, Inc., 1981.

(5) Antreich, K.J., and Koblitz, R.K., "Design Centering by Yield Prediction," IEEE Trans. on Circuits and Systems, Vol. CAS-29, No. 2, Feb. 1982.

(6) Voreadis, A., and Mayne, D.Q., "A Cut-Map Algorithm for Design Problems with Parameter Tolerances and Tuning," IEEE Trans. on Circuits and Systems, Vol. CAS-29, No. 5, May 1982.

(7) Elias, N.J., "New Statistical Methods for Assigning Device Tolerances," IEEE Proc. 1975 ISCAS.

(8) Bandler, J.W., "Optimization of Design Tolerances Using Non- Linear Programming," J. Optimiz. Theory Appl., Vol. 14, No. 1, July 1974.

(9) Bandler, J.W., Liu, P.C., and Tromp, H., "Non-Linear Programming Approach to Optimal Design Centering, Tolerancing, and Tuning," IEEE Trans. on Circuits and Systems, Vol. CAS-23, No. 3, March 1976.

(10) Singhal, K., and Pinel, J.F., "Statistical Design Centering and Tolerancing Using Parametric Sampling," IEEE Trans. on Circuits and Systems, Vo. CAS-28, No. 7, July 1981.

(11) R.S. Pengelly, Microwave Field Effect Transistors - Theory, Design and Applications, (Research Studies Press, Chichester, Eng., 1982), pg. 142.